Specifying and Verifying External Behaviour of Fair Input/Output Automata by Using the Temporal Logic of Actions

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Abstract. Fair input/output (or I/O) automata are a state-machine model for specifying and verifying reactive and concurrent systems. For the verification purposes, one is usually interested only in the sequences of interactions fair I/O automata offer to their environment. These sequences are called fair traces. The usual approach to the verification consists in proving fair trace inclusion between fair I/O automata. This paper presents a simple approach to the specification of fair traces and shows how to establish a fair trace inclusion relation for a pair of fair I/O automata by using the temporal logic of actions.

Key words: formal specification, fair input/output automaton, temporal logic of actions, fair trace, fair trace inclusion.

1. Introduction

Input/output automata (or I/O automata) are a popular set-theoretic model for the specification and analysis of reactive and concurrent systems (Tuttle, 1987; Lynch and Tuttle, 1989). They have, for example, been applied for reasoning about data communications protocols (Søgaard-Andersen et al., 1993), trust management systems (Krukow and Nielsen, 2007; Trček, 2014), Web services (Mitra et al., 2007), and database replication protocols (Armendáriz-Iñigo et al., 2009). An I/O automaton is a state machine in which each state transition is labelled by an action. Originally, no formal language for precise description of I/O automata system models and their correctness properties has been proposed. I/O automata have usually been described by using text and pseudocode. Preconditions and effects on variables introduced to represent automata states were specified for every possible action. The IOA programming language (Garland and Lynch, 2000) formalizes this semi-formal precondition/effect style. It is similar to the usual programming languages in that it has a reach formally defined syntax for the description of systems but cannot directly be used for reasoning about them. The reasoning has to be carried out by using its semantics written in a lower-level language of a theorem prover and in a specific first-order logical language developed by its authors (Garland et al., 2003).
In contrast to IOA and the mentioned lower-level languages, the temporal logic of
actions (TLA) (Lamport, 1994) is a logical language which can be used for writing a
system specification by directly describing the system’s execution semantics in a simple
way similar to the precondition/effect style. The formal specification as well as reasoning
about systems can be carried out in TLA. In Kapus (2002, 2005), we show how TLA
can be used for the formal specification of systems based on a model similar to the I/O
automaton one, but containing mobility and dynamic creation of components. TLA can
be used in a similar way for the ordinary I/O automaton model because the latter can be
treated as a special case of the former.

In this paper, we further investigate TLA as a formal language for I/O automata. De-
spite the term ‘actions’ in its name, the implicit underlying model of TLA is a simple
state machine with no action labels. In Kapus (2002, 2005), we use a special variable for
recording the actions in such a way that the TLA specification of a finite-state I/O automa-
ton may give infinitely many reachable states (here, in contrast to the formal definition for
TLA, by a ‘state’ we mean an assignment to a limited number of variables). The aim of
this paper are finite-state TLA specifications for finite-state I/O automata, so as to be able
to verify them automatically by using TLC, the model checker for specifications based on
TLA (TLA Toolbox, 2014).

Usually, only the external behaviour, i.e. the sequences of actions visible to the envi-
ronment, is of concern in the verification of I/O automata. In the mentioned papers, we do
not deal with the problem of how to specify only the external behaviour, and we consider
only the specification of safety properties (i.e. ‘what may happen’), but not the specific-
ification of liveness properties (i.e. ‘what must happen’). Besides, we do not consider the
verification.

In this paper, we consider so-called fair I/O automata (Müller, 1998), which allow the
specification of liveness, and propose a simple way to specify the external behaviour of
fair I/O automata, i.e. so-called traces and fair traces, by using TLA. The usual approach
to the verification of fair I/O automata consists in proving (fair) trace inclusion. We show
how a (fair) trace inclusion relation can be established for a pair of fair I/O automata by
using TLA.

The paper proceeds as follows. Section 2 briefly presents TLA. Section 3 contains the
necessary preliminaries about fair I/O automata. In Section 4, we present our approach to
the specification of fair traces by using TLA. In Section 5, we show how to verify (fair)
trace inclusion between fair I/O automata with TLA and give an example of using the TLC
model checker for this purpose. Section 6 contains a discussion and concludes this paper.

2. An Introduction to TLA

TLA is a simple linear-time temporal logic for specifying and reasoning about safety and
liveness of concurrent systems (Lamport, 1994). Besides other symbols, the language of
TLA contains a countably infinite set \( V \) of variables, partitioned into disjoint countably
infinite sets \( V_F \) and \( V_R \) of flexible and rigid variables (Merz, 2003). In the sequel, the
flexible variables will be called variables and the rigid ones constants, as in Lamport (1994, 2002). The language also contains a set Val of values, which is supposed to include different kinds of numbers, sets, strings, such as "CSZ", and similar. The semantics of TLA is defined in terms of behaviours, which are infinite sequences of states. A state is an assignment of values from Val to all the variables from $V_F$. The latter represent values that may change from state to state, whereas constants do not change their value. In the sequel, we will use $S_1$ to denote the set of all possible states and $s|_V$ to denote the restriction of a state $s$ to a set of variables $V \subset V_F$.

Temporal formulas of TLA, also called TLA formulas, are built from actions, Boolean operators, and temporal operators $\Box$ and $\exists$. No variable $v \in V_F$ should be of the form $v'$ because ' ("prime") is a special symbol of TLA, which can be applied to variables. Actions are first-order Boolean expressions which can contain values, constants, (unprimed) variables and primed variables. They are evaluated over pairs of states, called steps.

Informally, the unprimed variables denote their value in the 'current' state $s$ and the primed ones in the 'next' one, $t$, of a state pair $\langle s, t \rangle$. If $A$ is true in a state pair, the latter is called an A step. For example, action $y < 0 \land y' = y + 1$ informally says that $y < 0$ in the current state and that it is incremented by 1 in the next one. For $v$ a variable or a tuple of variables, $[A]_v$ is short for $A \lor \text{UNCHANGED } v$, and UNCHANGED $v$ means $v' = v$ ('applied to a tuple of variables is the same as applying it to each of them). $\langle A \rangle_v$ is short for $A \land (v' \neq v)$. A predicate $P$ is an action with no primed variables, with the consequence that it is true in a state pair $\langle s, t \rangle$ iff it is true in $s$. The predicate Enabled $A$ (read as action $A$ is enabled) is defined to be true in a state $s$ iff there exists such a state $t$ that $\langle s, t \rangle$ is an A step. For example, action $y < 0 \land y' = y + 1$ is enabled in every state in which $y < 0$.

The temporal formula $\Box F$ (read always $F$) is true of a behaviour iff $F$ is true of all its suffixes. $\Diamond F$ (read eventually $F$) is defined as $\neg \Box \neg F$. For $x$ a variable, $\exists x : F$ essentially means that there is some way of choosing a sequence of values for $x$ such that the temporal formula $F$ holds, but we do not care what these values are. It is said that $x$ is hidden in $F$. If $x$ is a tuple of variables $x_1, \ldots, x_n$, $\exists x : F$ is short for $\exists x_1 : \ldots : \exists x_n : F$.

For an action $A$, $WF_{vars}(A) \triangleq \Diamond (\Box A)_{vars} \lor \Box (\Diamond (\neg \text{Enabled}(A))_{vars})$ (triangle means 'by definition') specifies a weak fairness condition. It asserts that either action $(A)_{vars}$ occurs infinitely often during a behaviour or it is infinitely often disabled, or equivalently, that always, if action $(A)_{vars}$ is always enabled, it eventually occurs. $SF_{vars}(A) \triangleq \Diamond (\Box (A))_{vars} \lor \Diamond (\Diamond (\neg \text{Enabled}(A))_{vars})$ specifies a strong fairness condition. It asserts that either action $(A)_{vars}$ occurs infinitely often during a behaviour or it is disabled from some state on.

A temporal formula (or an action or a predicate) is said to be valid iff it is true of all possible behaviours (in all possible pairs of states or, respectively, in all states).

Most system specifications can be written as a 'canonical-form' TLA formula $\exists x : Init \land \Box [\text{Next}]_{vars} \land \text{Liveness}$ (Lamport, 2002), where $Init$ is a predicate, $\text{Next}$ an action (usually a disjunction of actions), $vars$ a tuple of variables the system may change, $x$ a tuple consisting of some of the variables from $vars$ (e.g. 'internal' variables of the system), and Liveness a conjunction of fairness conditions on (some disjuncts of) $\text{Next}$. Informally, a behaviour satisfies this formula iff it is possible to choose the values for $x$ such that $Init$
is true for the initial state, every pair of consecutive states is a $[\text{Next}]_{\text{vars}}$ step and the behaviour satisfies Liveness.

Suppose that we would like to specify a program (i.e. its runs) which operates on variables $x$ and $y$. Suppose that they have already been initialised to 0 during their definition in the program and that the rest of the code consists of the following sequence of statements: \( x = x + 1; \ y = y + 1 \). Therefore, it is expected to have a single program run—the following sequence of states: \( (x = 0, y = 0), (x = 1, y = 0), (x = 1, y = 1) \). As TLA is defined to specify infinite sequences of states, it can actually be used for the specification of this run with infinitely many states \( (x = 1, y = 1) \) added at the end. The TLA specification could be as follows (cf. Lamport, 1994):

\[
\exists pc : (pc = 0) \land (x = 0) \land (y = 0) \land [\text{Next}]_{\text{vars}} \land WF_{\text{vars}}(\text{Next}),
\]

where $vars \triangleq (pc, x, y)$ and $\text{Next} \triangleq ((pc = 0) \land (pc' = 1) \land (x' = x + 1) \land \text{UNCHANGED } y) \lor ((pc = 1) \land (pc' = 2) \land (y' = y + 1) \land \text{UNCHANGED } x)$.

A ‘program counter’ variable is introduced and hidden because it serves as an auxiliary variable in order to be able to properly specify the changes of $x$ and $y$. The specification allows behaviours which exactly agree with the program run in variables $x$ and $y$: in the initial state $x$ and $y$ are equal to 0, in the next state $x$ becomes equal to 1, in the state following this one $y$ becomes equal to 1, and in all the subsequent states they remain equal to 1. The weak fairness condition assures that behaviours in which both $x$ and $y$ always remain equal to 0 or $y$ does are not allowed. However, notice that the specification allows behaviours in which $x$ is not incremented immediately after the initial state and behaviours in which $y$ is not incremented immediately after the change of $x$. This is because TLA is unable to specify the exact state at which an enabled action (i.e. a state change) must occur. It can only specify that it eventually occurs. By definition, every TLA formula allows stuttering steps.

Formally, a step \( (s, t) \) is called a $V$-stuttering (or stuttering if $V$ is evident from the context) step iff \( s|y = t|y \), i.e. iff $s$ and $t$ are $V$-equivalent (meaning that they assign the same values to the variables in $V$). A behaviour is called $V$-stuttering free iff it does not contain $V$-stuttering steps except possibly at the end. Two behaviours are said to be $V$-stuttering equivalent iff they differ only in the number of consecutive $V$-equivalent states. TLA formulas are stuttering-invariant, which means the following. Suppose that $F$ is a TLA formula and $V$ the set of its free variables, such as, for instance, the set \( \{x, y\} \) in the program specification given in the above example. $F$ cannot distinguish between $V$-stuttering equivalent behaviours.

Notice that formulas of the form $\square[\text{Next}]_{\text{vars}}$, are stuttering-invariant because they allow $vars$-stuttering steps. Let us stress that formulas of the form $\exists x : F$ are also stuttering-invariant (Lamport, 1994). For example, the program specification given above does not distinguish between behaviours which differ only in the number of consecutive states in which $x$ and $y$ do not change. It follows that it does not specify only the behaviours that directly correspond to the program run in $x$ and $y$, but also the behaviours that are \( \{x, y\}\)-stuttering equivalent to them, i.e. it specifies an equivalence class.

If $F$ is a TLA formula specifying a system and $G$ one specifying a property, the system has that property iff the implication $F \Rightarrow G$ is valid. For any TLA formulas $F$ and $G$, if $x$, $y$ are tuples of variables, the implication $(\exists x : F) \Rightarrow (\exists y : G)$ can be proved by exhibiting
the validity of $F \Rightarrow \overline{G}$, where $\overline{G}$ is obtained by substituting $\overline{y}$ for the free occurrences of $y_i$ in $G$ for all $i$. Each $\overline{y}$ is a function of variables that occur in $F$. The functions are collectively called a refinement mapping.

3. Fair I/O Automata

We consider the kind of I/O automaton model called fair I/O automaton (Müller, 1998) in order to be able to specify systems with the help of fairness conditions as with many specification formalisms (Romijn and Vaandrager, 1996), including TLA. In this section, let us temporarily forget about TLA and look at the I/O automata terminology (cf. Müller, 1998; Søgaard-Andersen et al., 1993; Tuttle, 1987).

**Definition 1.** A fair I/O automaton $A$ consists of the following components:

- An action signature $\text{sig}(A) = (\text{in}(A), \text{out}(A), \text{int}(A))$ consisting of disjoint sets of input, output, and internal actions, respectively. $\text{ext}(A)$ denotes the set $\text{in}(A) \cup \text{out}(A)$ of external actions, $\text{local}(A)$ the set $\text{out}(A) \cup \text{int}(A)$ of locally controlled actions, and $\text{acts}(A)$ the set $\text{ext}(A) \cup \text{int}(A)$ of all actions.
- A set $\text{states}(A)$ of states.
- A nonempty set $\text{start}(A)$ of start states ($\text{start}(A) \subseteq \text{states}(A)$).
- A transition relation $\text{steps}(A) \subseteq \text{states}(A) \times \text{acts}(A) \times \text{states}(A)$. The transition relation $\text{steps}(A)$ must have the property that for each state $s \in \text{states}(A)$ and each input action $a \in \text{in}(A)$ there exists a state $s' \in \text{states}(A)$ such that $(s, a, s') \in \text{steps}(A)$.
- Sets $w\text{fair}(A)$ and $s\text{fair}(A)$ of weak fairness sets and strong fairness sets, respectively, which are subsets of $\text{local}(A)$.

In the sequel, by I/O automata we will mean fair I/O automata unless being evident from the context that we mean otherwise. A (fair) I/O automaton with empty sets $w\text{fair}(A)$ and $s\text{fair}(A)$ is called safe I/O automaton. For $A$ a fair I/O automaton, let $\text{safe}(A)$ denote the safe I/O automaton obtained from $A$ by setting $w\text{fair}(A)$ and $s\text{fair}(A)$ to empty sets.

An action $a$ is enabled in a state $s$ if there exists a state $s'$ such that $(s, a, s') \in \text{steps}(A)$. A set $\mathcal{A}$ of actions is said to be enabled in state $s$ if there exists an action $a \in \mathcal{A}$ such that $a$ is enabled in $s$. An action or set of actions which is not enabled in a state $s$ is said to be disabled in $s$.

An execution $\alpha$ of an I/O automaton $A$ is a finite or infinite sequence $\alpha = \langle s_0, a_1, s_1, \ldots \rangle$ of alternating states and actions of $A$ beginning with a state, and if it is finite, also ending with a state, such that $s_0 \in \text{start}(A)$ and for all $i$, $(s_i, a_{i+1}, s_{i+1}) \in \text{steps}(A)$. The set of all executions of $A$ is denoted by $\text{execs}(A)$. A state $s$ of $A$ is reachable if there exists a finite execution of $A$ that ends in $s$.

The trace of an execution $\alpha$ is the subsequence of $\alpha$ consisting of all the external actions of $A$, i.e. the restriction of sequence $\alpha$ to the elements of $\text{ext}(A)$. For example, if $\alpha = \langle s_0, a_1, s_1, a_2, s_2, a_3, s_3 \rangle$ and only $a_1$ and $a_3$ are external actions, then its trace is the sequence $\langle a_1, a_3 \rangle$. We say that $\gamma$ is a trace of $A$ if there exists an execution $\alpha$ of $A$ such that $\gamma$ is the trace of $\alpha$. The set of all traces of $A$ is denoted by $\text{traces}(A)$. 
An execution $\alpha$ of a fair I/O automaton $A$ is weakly fair if the following conditions hold for each $W \in wfair(A)$:

1. If $\alpha$ is finite, then $W$ is not enabled in the last state of $\alpha$.
2. If $\alpha$ is infinite, then either $\alpha$ contains infinitely many occurrences of actions from $W$, or $\alpha$ contains infinitely many occurrences of states in which $W$ is disabled.

An execution $\alpha$ of $A$ is strongly fair if the following conditions hold for each $S \in sfair(A)$:

1. If $\alpha$ is finite, then $S$ is not enabled in the last state of $\alpha$.
2. If $\alpha$ is infinite, then either $\alpha$ contains infinitely many occurrences of actions from $S$, or $\alpha$ contains only finitely many occurrences of states in which $S$ is enabled.

An execution $\alpha$ is fair if it is both weakly and strongly fair. The set of all fair executions of $A$ is denoted by $faireックス(A)$. The set of all traces originating from the fair executions of $A$ is denoted by $fairtraces(A)$. For safe I/O automata, the notions of executions (respectively traces) and fair executions (respectively fair traces) coincide.

For $A$ a fair I/O automaton, it is desirable that $safe(A)$ alone specify the safety properties of $A$, i.e. that these are completely determined by $execs(A)$. Sets $wfair(A)$ and $sfair(A)$ should only specify the liveness properties of $A$, i.e. it should be possible to extend every finite execution of $A$ to a fair execution of $A$. Additionally, it should be possible to do that independently of the inputs provided by the environment of $A$ (Romijn and Vaandrager, 1996). In the literature (e.g. Segala et al., 1998), a pair $(B, L)$ consisting of a safe I/O automaton $B$ and a set $L \subseteq execs(B)$ such that $B$ can always generate an execution in $L$ independently of the environment is called a live I/O automaton.

**Definition 2.** (Cf. Müller, 1998.) Let $A$ be a fair I/O automaton and $\Lambda$ a subset of its locally controlled actions. $\Lambda$ is input-resistant iff for each pair of reachable states $s, t$ and each input action $a$, if $\Lambda$ is enabled at $s$ and $(s, a, t) \in steps(A)$, then $\Lambda$ is enabled at $t$. A fair I/O automaton is said to be input-resistant if every set in $sfair(A)$ is input-resistant.

Romijn and Vaandrager (1996) prove that if a fair I/O automaton $A$ is (i) input-resistant and (ii) at most countably many sets in $wfair(A) \cup sfair(A)$ are enabled in each reachable state of $A$, then $A$ induces live automaton $live(A) = (safe(A), faireックス(A))$.

We are interested in the verification of I/O automata by using implementation relations. Fair I/O automata which induce live I/O automata can be verified by using the following ones.

**Definition 3.** (Cf. Søgaard-Andersen et al., 1993; Müller, 1998.) Let $A$ and $B$ be fair I/O automata with $in(A) = in(B)$ and $out(A) = out(B)$, such that they induce live automata $live(A) = (safe(A), faireックス(A))$ and, respectively, $live(B) = (safe(B), fareックス(B))$. There is a safe trace inclusion, written as $A \preceq_s B$, iff $traces(A) \subseteq traces(B)$. There is a fair trace inclusion, written as $A \preceq_f B$, iff $fairtraces(A) \subseteq fairtraces(B)$.

Clearly, for safe I/O automata, the safe and fair trace inclusion relations coincide.
4. Specification of Fair Traces with TLA

As the meaning of TLA is only defined for infinite (state) sequences, let us make all the finite executions of an I/O automaton $A$ infinite as in Søgaard-Andersen et al. (1993). Let $\zeta$ denote a special stuttering action and suppose that it cannot be in the action signature of any automaton. A stuttering step is any triple of the form $(s, \zeta, s)$, where $s$ is a state. For any execution $\alpha = \langle s_0, a_1, s_1, \ldots \rangle$, let the extended execution $\hat{\alpha} \triangleq \alpha$ if $\alpha$ is infinite, and $\hat{\alpha} \triangleq \langle s_0, a_1, s_1, \ldots, a_n, s_n, \zeta, s_n, \zeta, s_n, \ldots \rangle$ if $\alpha$ is finite and ends in $s_n$. Analogously, for any trace, we define the extended trace to be the same if it is infinite, and obtained by adding infinitely many stuttering actions at the end of it if finite.

There is obviously a one-to-one correspondence between the set $\text{execs}(A)$ and the set of extended executions obtained from the executions in $\text{execs}(A)$. This is because all the infinite executions remain intact and, by definition, do not contain stuttering steps, whereas every finite execution only gets the stuttering steps at the end. It can also be proved (cf. Søgaard-Andersen et al., 1993) that for all finite executions $\alpha$, $\alpha$ satisfies the weak (respectively strong) fairness conditions as defined for finite executions exactly if $\hat{\alpha}$ satisfies the weak (respectively strong) fairness conditions as defined for infinite executions. Therefore, there is also a one-to-one correspondence between the set $\text{fairexecs}(A)$ and the set of fair executions in the set of extended executions of $A$.

Let the definitions of traces of the extended executions of $A$ remain the same as for the original executions, by $\zeta$ treated as an external action, except for the extended executions which contain only steps with internal actions at the end. Since for such an execution, the original definition of traces gives a finite action sequence, the infinite number of stuttering actions $\zeta$ must be added at its end. Obviously, the traces of previously finite executions contain the infinite number of actions $\zeta$ at the end. There is, evidently, a one-to-one correspondence between the original set of (fair) traces, the set of (fair) extended traces and the set of (fair) traces obtained from the set of extended (fair) executions of $A$. In the sequel, we will, therefore, identify (the notations for) (fair) executions and, respectively, traces with (the notations for) their extended versions. Clearly, the definitions of both implementation relations remain valid.

From this point on, we can proceed with the preparation of TLA specifications of I/O automata in a similar way to how TLA is used for specifying program runs (e.g. Lamport, 1994; Reynolds, 1998). It means that the TLA specifications will not specify exactly the (extended) executions or traces of I/O automata, but the union of their equivalence classes, where for every execution (and consequently every trace), its equivalence class will contain, besides it, all the executions (respectively traces) which can be obtained from it by adding finitely many stuttering steps at some states (respectively stuttering actions after some actions). And, most importantly, all the results of reasoning about such TLA specifications will be valid for the original executions or traces.

4.1. Specification of Executions

We will first explain the specification of executions of an I/O automaton with help of an example. Let us write the TLA specification of $\text{execs}(A_1)$ for I/O automaton $A_1$ with
Examples of executions of A can be denoted by TLA values \( s \) specifying states in a similar way to the program statements in the example in Section 2. However, the action labels \( a \) currently enabled transition of the automaton occurs. If the latter is the case, the first \( Ev = \langle a \rangle \) and \( Act(Ev, v) \models Ev' = \langle if Ev[1] = "0" then "1" else "0", v \rangle \).

We need to represent the states with a TLA variable. Let it be \( st \) its value "\( s0 \)" or "\( s1 \)" or "\( s2 \)" representing states \( s0, s1, s2 \) respectively. We can specify the transitions between states in a similar way to the program statements in the example in Section 2. However, the specification also has to represent the action labels of the transitions. Let the action labels be denoted by TLA values "\( a \)" "\( b \)" and "\( c \)". We introduce a special variable \( Ev \) in which we record the action label of the transition being specified. In the sequel, let \( ActInit(Ev) \models Ev = \langle "0", \langle \rangle \rangle \) and \( Act(Ev, v) \models Ev' = \langle if Ev[1] = "0" then "1" else "0", v \rangle \).

The TLA specification of \( execs(A1) \) can then be written as follows:

\[
SpecE(st, Ev) \models Init(st, Ev) \land \square Next(st, Ev) vars
\]

where

\[
vars \models (st, Ev)
\]

\[
Init(st, Ev) \triangleq Init(st) \land ActInit(Ev)
\]

\[
InActionA(st, Ev) \triangleq Act(Ev, \"a\") \land (st' = if st = "s0" then "s1" else st)
\]

\[
OutActionC(st, Ev) \triangleq Act(Ev, \"c\") \land (st = "s1") \land (st' = "s2")
\]

\[
IntActionB(st, Ev) \triangleq Act(Ev, \"b\") \land (st = "s1") \land \text{UNCHANGED st}
\]

\[
Next(st, Ev) \triangleq InActionA(st, Ev) \lor OutActionC(st, Ev) \lor IntActionB(st, Ev)
\]

The TLA action \( InActionA(st, Ev) \) represents the transitions from Fig. 1 labelled with action \( a \), action \( OutActionC(st, Ev) \) represents the transition labelled with \( c \), and action \( IntActionB(st, Ev) \) the transition labelled with \( b \).

\( SpecE(st, Ev) \) says that initially, \( st \) is set to "\( s0 \)" and \( Ev \) is equal to the pair of values \( \langle "0", \langle \rangle \rangle \), and that subsequently, at every step, either both \( st \) and \( Ev \) remain unchanged or a currently enabled transition of the automaton occurs. If the latter is the case, the first
component of \( Ev \), denoted \( Ev[1] \), changes to “1” if previously “0”, and vice versa, and in the second component of \( Ev \), denoted \( Ev[2] \), the label of the transition is recorded. For example, in the initial state, only the TLA action \( InActionA(st, Ev) \) is enabled. If it occurs, \( Ev \) becomes equal to \((“1”, (“a”))\) and \( st \) to “s1”, which represents the execution of the transition from \( s0 \) to \( s1 \).

We want to recognise from the \( Ev \) variable alone whether an I/O automaton action occurred. That is why we defined \( Act(Ev, v) \) to unconditionally change \( Ev \). If only the action were recorded in \( Ev \), i.e. if \( Act(Ev, v) \) were defined as \( Ev’ = v \), the repetition of an action could not be distinguished from stuttering in \( Ev \). For example, the sequence of values of \( Ev \) in the behaviour representing execution \( ⟨s0, a, s1⟩ \) and respectively \( ⟨s0, a, s1, a, s1⟩ \) would be the same: \( ⟨∅, (“a”), (“a”), . . .⟩ \). For our definition of \( Act(Ev, v) \), it is \( ⟨(“0”, ∅), (“1”, (“a”)), (“1”, (“a”)), . . .⟩ \) for the first execution and \( ⟨(“0”, ∅), (“1”, (“a”)), (“0”, (“a”)), (“0”, (“a”)), . . .⟩ \) for the second one.

Let \( A \) denote a fair I/O automaton (Definition 1), \( V \) the set of TLA variables encoding the automaton states, and \( Ev \) a TLA variable different from those from \( V \). From the above example, it can easily be seen that generally, a TLA specification of \( execs(A) \) can be written as follows:

\[
Init(V, Ev) \land \Box[Next(V, Ev)]_{[V, Ev]}
\]  

(1)

where

- \( Init(V, Ev) \triangleq StInit(V) \land ActInit(Ev) \) with \( StInit(V) \) a TLA predicate such that for all \( s \in St \), it is true in \( s \) iff \( s|_{V} \in start(A) \), and
- \( Next(V, Ev) \triangleq \bigvee_{a \in act(A)} Next_a(V, Ev) \) with \( Next_a(V, Ev) \triangleq NState_a(V) \land Act(Ev, a) \), where \( NState_a(V) \) is a TLA action such that for all \( s, t \in St \), \( NState_a(V) \land Act(Ev, a) \) is true in \( ⟨s, t⟩ \) iff \( ⟨s|_{V}, a, t⟩ \in steps(A) \).

\( StInit(V) \) specifies the initial states of \( A \), and \( Next_a(V, Ev) \) describes all the possible transitions labelled by \( a \). The \([V, Ev] \) stuttering steps represent the stuttering steps as defined for I/O automata. Please, note that the restriction to \( V \) has to be applied to the states of TLA behaviours in order to obtain the corresponding states of \( A \) because the states in TLA assign values to all the variables of TLA. It follows that one execution of \( A \) is in fact represented by the set of all the TLA behaviours which agree with the execution in the values of \( V \) and in the actions recorded in \( Ev \), but assign arbitrary values to all the other variables. For the simplicity of writing, we sometimes ignore this fact as usual in papers on TLA.

### 4.2. Specification of Fair Executions

In TLA, an occurrence of action \( a \) of a fair I/O automaton \( A \) can be expressed by \( ⟨Next_a(V, Ev)⟩_{[V, Ev]} \) (which happens to be equivalent to \( Next_a(V, Ev) \)). It can easily be seen that the enabledness of action \( a \) in a state of \( A \) can be expressed with the \( Enabled \) predicate. Formally, for all \( s \in St \), if \( s|_{V} \in states(A) \), then \( Enabled(Next_a(V, Ev))_{[V, Ev]} \)
is true in \( s \) iff action \( a \) is enabled in state \( s|_V \). The conjunct \( \text{Act}(Ev, a) \) in \( \text{Next}_a(V, Ev) \) ensures that this is the case even if the transition relation of \( A \) contains steps \((s|_V, a, s|_V)\) for some \( a \) and \( s \).

Consequently, the TLA specification of \( \text{fairexecs}(A) \) can be obtained by adding weak and strong fairness conditions to (1):

\[
\text{Init}(V, Ev) \land \Box [\text{Next}(V, Ev)](V, Ev) \land \text{Liveness}(V, Ev) \tag{2}
\]

where \( \text{Liveness}(V, Ev) \triangleq \land_{W \in \text{wfair}(A)} \text{WF}_{(V, Ev)}(\lor_{a \in W} \text{Next}_a(V, Ev)) \land \land_{S \in \text{sfair}(A)} \text{SF}_{(V, Ev)}(\lor_{a \in S} \text{Next}_a(V, Ev)). \)

\( V \) and \( Ev \) in the parentheses in the above introduced symbols (and similar in the rest of the paper) denote the free variables of the formulas they represent. Please, observe that instead of writing \( V \) in the parentheses and in the subscripts such as \( \langle V, Ev \rangle \), we should list the variables of \( V \). We write \( V \) for convenience.

Notice that the set \( \text{wfair}(A_1) \) of our example automaton \( A_1 \) is nonempty. The TLA specification of \( \text{fairexecs}(A_1) \) can be written by adding the fairness condition to the specification of \( \text{execs}(A_1) \):

\[
\text{SpecFE}(st, Ev) \triangleq \text{SpecE}(st, Ev) \land \text{Liveness}(st, Ev)
\]

where

\[
\text{Liveness}(st, Ev) \triangleq \text{WF}_{\text{vars}}(\text{OutActionC}(st, Ev)) \lor \text{IntActionB}(st, Ev)).
\]

Examples of fair executions of \( A_1 \) are \( \langle s_0 \rangle, \langle s_0, a, s_1, c, s_2 \rangle, \langle s_0, a, s_1, a, s_1, c, s_2 \rangle, \langle s_0, a, s_1, b, s_1, b, s_1, c, s_2 \rangle, \langle s_0, a, s_1, b, s_1, b, s_1, \ldots \rangle \) (i.e. an infinite execution in which action \( b \) is repeated indefinitely in state \( s_1 \)), but not for instance \( \langle s_0, a, s_1 \rangle \), because \( b \) and \( c \), which are together in a set of \( \text{wfair}(A_1) \), are enabled in the last state.

4.3. Specification of Traces

Now, we are interested in writing the TLA specification of traces of a fair I/O automaton \( A \). The only free variable of the specification should be one in which only the occurrences of the external actions of \( A \) would be recorded (we shall call it \( Ev \) as before), thus representing traces, and the specification should be stuttering-invariant. If \( A \) has no internal actions, the specification can be obtained by hiding the variables representing its states in the TLA specification of its executions (1) by using \( \exists \). If not, the specification of \( \text{traces}(A) \) can be written in the same way as (1), except that in the definition of \( \text{Next}_a(V, Ev) \) for every internal action \( a, Ev \) should remain unchanged, i.e. the occurrence of \( a \) should not be recorded in \( Ev \), and \( V \) should finally be hidden:

\[
\exists V : \text{Init}(V, Ev) \land [\text{Next}_H(V, Ev)](V, Ev) \tag{3}
\]
where \( \text{NextH}(V, Ev) \triangleq \bigvee_{a \in \text{ext}(A)} \text{Next}_a(V, Ev) \lor \bigvee_{a \in \text{int}(A)} \text{Next}_a(V, Ev) \) with \( \text{Next}_a(V, Ev) \triangleq \text{NState}_a(V) \land \text{Act}(Ev, a) \) for all \( a \in \text{ext}(A) \) and \( \text{Next}_a(V, Ev) \triangleq \text{NState}_a(V) \land Ev' = Ev \) for all \( a \in \text{int}(A) \).

For our example automaton \( A \), the specification of traces is as follows:

\[
\text{SpecT}(Ev) \triangleq 3 \text{st} : \text{Init}(st, Ev) \land \square[\text{NextH}(st, Ev)]_{\text{vars}}
\]

where

\[
\text{vars} \triangleq \langle st, Ev \rangle
\]

\[
\text{StInit}(st) \triangleq st = "s0"
\]

\[
\text{Init}(st, Ev) \triangleq \text{StInit}(st) \land \text{ActInit}(Ev)
\]

\[
\text{InActionA}(st, Ev) \triangleq \text{Act}(Ev, \langle "\text{a}\rangle \rangle) \land (st' = \text{if } st = "s0" \text{ then } "s1" \text{ else } st)
\]

\[
\text{OutActionC}(st, Ev) \triangleq \text{Act}(Ev, \langle "\text{c}\rangle \rangle) \land (st = "s1") \land (st' = "s2")
\]

\[
\text{IntActionBH}(st, Ev) \triangleq (st = "s1") \land \text{UNCHANGED } \langle st, Ev \rangle
\]

\[
\text{NextH}(st, Ev) \triangleq \text{InActionA}(st, Ev) \lor \text{OutActionC}(st, Ev) \lor \text{IntActionBH}(st, Ev)
\]

Notice that instead of the TLA action \( \text{IntActionBH}(st, Ev) \), the specification contains the TLA action \( \text{IntActionBH}(st, Ev) \), which does not record the occurrence of action \( b \) in \( Ev \). Examples of traces of \( A \) are \( \langle \rangle \), \( \langle a \rangle \), \( \langle a, a \rangle \), \( \langle a, a, \ldots \rangle \), \( \langle a, c \rangle \).

### 4.4. Specification of Fair Traces

Clearly, if a fair I/O automaton \( A \) does not contain internal actions, the specification of its fair traces can be obtained by hiding \( V \) in the specification of its fair executions.

Otherwise, following the way the specification of \( \text{fairexecs}(A) \) (2) was obtained from the specification of \( \text{execs}(A) \) (1), one is tempted to write the specification of \( \text{fairtraces}(A) \) by adding the fairness conditions for the TLA actions that represent fairness sets from \( \text{wfair}(A) \) and \( \text{sfair}(A) \) to (3):

\[
\exists V : \text{Init}(V, Ev) \land \lbrack \text{NextH}(V, Ev) \rbrack_{V,Ev} \land \text{LivenessH}(V, Ev)
\] (4)

where \( \text{LivenessH}(V, Ev) \triangleq \bigwedge_{W \in \text{wfair}(A)} \text{WF}_{V,Ev}(\bigvee_{a \in W} \text{Next}_a(V, Ev)) \land \bigwedge_{S \in \text{sfair}(A)} \text{SF}_{V,Ev}(\bigvee_{a \in S} \text{Next}_a(V, Ev)) \).

It should, however, be noticed that the transition relation of an I/O automaton \( A \) may contain steps \((s, a, s)\) for some \( a \in \text{acts}(A) \) and \( s \in \text{states}(A) \). It follows that \( \text{NState}_a(V) \) does not necessarily change \( V \). In (1) and (2), the I/O automaton transitions are represented by \( \text{Next}_a(V, Ev) \) in which the conjunct \( \text{Act}(Ev, a) \) guarantees that the state in TLA changes for every I/O automaton step. In (3) and consequently in (4), this is not the case anymore, as we leave \( Ev \) unchanged in \( \text{Next}_a(V, Ev) \) for all \( a \in \text{int}(A) \).

Reynolds (1998) shows that if some TLA actions do not always change the state, it can happen that the canonical-form TLA specification including weak and/or strong fairness
conditions on such actions does not specify all the behaviours of the system being specified. Some legal behaviours of the system might not be allowed by the specification as not being weakly or strongly fair.

This would, for instance, be the case for our example automaton $A_1$. Following (4), the liveness specification $LivenessH(V, Ev)$ for $A_1$ would be:

$$WF_{[st, Ev]}(OutActionC(st, Ev) \lor IntActionBH(st, Ev))$$

(5)

which is defined as

$$\forall \Box \Diamond (OutActionC(st, Ev) \lor IntActionBH(st, Ev))_{[st, Ev]}$$

$$\forall \Box \Diamond (\neg \text{Enabled} (OutActionC(st, Ev) \lor IntActionBH(st, Ev))_{[st, Ev]}).$$

As $IntActionBH(st, Ev)$ does change neither $st$ nor $Ev$, $(OutActionC(st, Ev) \lor IntActionBH(st, Ev))_{[st, Ev]}$ is equivalent to $(OutActionC(st, Ev))_{[st, Ev]}$, giving that (5) is equivalent to $WF_{[st, Ev]}(OutActionC(st, Ev))$, which expresses a stronger weak fairness condition than defined by $wfair(A)$. So, for instance, from the fair execution $(s0, a, s1, b, s1, b, s, \ldots)$ of $A_1$, we obtain fair trace $(a)$, but it is not allowed by the specification of the form (4) for this automaton because it does not satisfy the weak fairness condition (5). The latter namely requires that if $c$ is always enabled from some state on (note that this is the case if only $b$ is executed all the time after reaching $s1$ from $s0$), it must eventually occur.

Therefore, the specification of fair traces in the form (4) is generally possible only under the condition that for all $W \in wfair(A)$ and $S \in sfair(A)$, for all $a \in W \cap int(A)$ and, respectively, for all $a \in S \cap int(A)$, $NState_a(V)$ (or more precisely, $NState_a(V) \cap T$ where $T$ is the type invariant for $V$) implies $V' \neq V$, i.e. that all the TLA actions representing the internal actions of $A$ for which fairness conditions are imposed, change some variable of the specification other than $Ev$.

Nevertheless, we would like to have a generally valid pattern for the specification of fair traces. We have found that it is possible to apply a solution similar to the one proposed by Reynolds (1998) for the specification of concurrent programs based on multiset rewriting. Instead of the TLA formulae of the form $WF_{vars}(A)$ and $SF_{vars}(A)$, the TLA formulae of the form $VWF_{vars}(A)$ and $ASF_{vars}(A)$ introduced by Reynolds (1998) should be used for the specification of fairness sets.

$VWF_{vars}(A)$ expresses very weak fairness:

$$VWF_{vars}(A) \triangleq WF_{vars}(A) \lor \Box \Diamond \text{Enabled} (A \land vars' = vars).$$

$ASF_{vars}(A)$ expresses almost strong fairness:

$$ASF_{vars}(A) \triangleq SF_{vars}(A) \lor \Box \Diamond \text{Enabled} (A \land vars' = vars).$$

The specification of fair traces of any fair I/O automaton $A$ can be obtained from the specification of traces (3) in a uniform way. It can be written in the same form as (4), but $LivenessH(V, Ev)$ has to be as follows:

$$LivenessH(V, Ev) \triangleq \land_{W \in wfair(A)} VWF_{[V, Ev]}(\bigvee_{a \in W} \text{Next}_a(V, Ev))$$

$$\land_{S \in sfair(A)} ASF_{[V, Ev]}(\bigvee_{a \in S} \text{Next}_a(V, Ev)).$$
Let us remark that it is not necessary to apply the new version of fairness conditions for fairness sets $W$ and $S$ which do not contain internal actions $a$ labelling steps $(s, a, s)$ for some states $s$. However, instead of checking as to whether such actions exist, it is generally easier to use the new versions for all the fairness sets. The new fairness conditions for fairness sets $W$ and $S$ which do not contain the critical internal actions are, anyway, equivalent to the old ones.

We will demonstrate in Section 5 that by using the new form of fairness conditions we obtain a proper TLA specification of the fair traces of our example automaton $A1$. Its fairness part should be:

$$Liveness_{H}(st, Ev) \triangleq WF_{(st, Ev)}(OutActionC(st, Ev) \lor IntActionB(st, Ev)) \lor \Box \Diamond \text{Enabled} (\Box OutActionC(st, Ev) \lor IntActionBH(st, Ev) \land (st, Ev)' = (st, Ev))$$

which is equivalent to

$$WF_{(st, Ev)}(OutActionC(st, Ev)) \lor \Box \Diamond \text{Enabled} (IntActionBH(st, Ev)).$$

5. Fair I/O Automata Implementation Relations in TLA

Suppose that $Tr_A(Ev)$ and $FTr_A(Ev)$ denote TLA specifications of traces and, respectively, fair traces of an I/O automaton $A$. Analogous to the (fair) executions of an I/O automaton $A$, since the states in TLA are assignments to all the variables in $V_F$, not only to $Ev$, one (fair) trace of an I/O automaton has a set of representative behaviours that satisfy the TLA specification of the (fair) traces of $A$. This set contains all the $Ev$-stuttering free behaviours with the values of $Ev$ corresponding to the actions in the (fair) trace and all the behaviours which are $Ev$-stuttering equivalent to them. For a trace $\alpha$, let this set (the ‘equivalence class’ for $\alpha$) be denoted by $\text{equ}_{Ev}(\alpha)$. For a behaviour $\sigma$ and a TLA formula $F$, let $\sigma \models F$ denote that $F$ is true of $\sigma$.

**Proposition 1.** For fair I/O automata $A$ and $B$ with $in(A) = in(B)$ and $out(A) = out(B)$ which induce the corresponding live automata, $A \preceq_F B$ iff $FTr_A(Ev) \Rightarrow FTr_B(Ev)$ is valid.

**Proof.**

$\Rightarrow$:
Assume that $A \preceq_F B$. Hence, by Definition 3, $\text{fairtraces}(A) \subseteq \text{fairtraces}(B)$, and so for every $\alpha \in \text{fairtraces}(A)$, $\alpha \in \text{fairtraces}(B)$. For a behaviour $\sigma$, assume that $\sigma \models FTr_A(Ev)$. We must prove that $\sigma \models FTr_B(Ev)$. We know that $\sigma \in \text{equ}_{Ev}(\alpha)$ for some $\alpha \in \text{fairtraces}(A)$. We know that $\alpha \in \text{fairtraces}(B)$ and that all the behaviours in $\text{equ}_{Ev}(\alpha)$ satisfy $FTr_B(Ev)$. Henceforth, $\sigma \models FTr_B(Ev)$.

$\Leftarrow$:
Assume the validity of $FTr_A(Ev) \Rightarrow FTr_B(Ev)$. Hence, for every $\sigma$ such that $\sigma \models FTr_A(Ev)$, $\sigma \models FTr_B(Ev)$. Assume that $\alpha \in \text{fairtraces}(A)$. We must prove that $\alpha \in$
We know that for all $\sigma \in \text{equ}_{\text{Ev}}(\alpha)$, $\sigma \models F\text{Tr}_{A}(\text{Ev})$ and thus $\sigma \models F\text{Tr}_{B}(\text{Ev})$. It follows that $\sigma \in \text{equ}_{\text{Ev}}(\beta)$ for some $\beta \in \text{fairtraces}(B)$. From the fact that $\sigma$ cannot be in the equivalence classes for two different fair traces, it follows that $\alpha = \beta$ and hence, $\alpha \in \text{fairtraces}(B)$. □

**Proposition 2.** For fair I/O automata $A$ and $B$ with $\text{in}(A) = \text{in}(B)$ and $\text{out}(A) = \text{out}(B)$ which induce the corresponding live automata, $A \preceq B$ iff $\text{Tr}_{A}(\text{Ev}) \Rightarrow \text{Tr}_{B}(\text{Ev})$ is valid.

**Proof.** Analogous to the proof of Proposition 1, or by the latter by taking into account that $\text{traces}(A) = \text{fairtraces}(\text{safe}(A))$ and the same for $B$. □

We would also like to be able to check whether a fair I/O automaton $A$ induces a live automaton by using TLA. Suppose that a TLA specification of $\text{fairexecs}(A)$ in the form (2) is given. We are only interested in automata with countable (i.e. finite or countably infinite) sets $\text{sfair}(A)$ and $\text{wfair}(A)$ as is regularly the case in the literature (e.g. Müller, 1998; Søgaard-Andersen et al., 1993). For such automata, the liveness part $\text{Liveness}(V, \text{Ev})$ is a conjunction of countably many fairness conditions. As the countable sets of fairness sets of $A$ imply condition (ii) of Romijn and Vaandrager (1996) mentioned in Section 3, it follows that in order to assure that $A$ induces a live automaton, it is only necessary to check whether it is input-resistant. Let $S_A$ denote the TLA specification of $\text{execs}(A)$ (1). Based on Definition 2 and the semantics of TLA we claim that $A$ is input-resistant iff formula

$$S_A(V, \text{Ev}) \Rightarrow [\neg (A \triangleq \bigvee a \in S \text{Next}_a(V, \text{Ev})) \land \text{ENABLED}(A)_{(V, \text{Ev})}] \Rightarrow [\text{ENABLED}(A)_{(V, \text{Ev})}]$$

is valid for every action $A \triangleq \bigvee a \in S \text{Next}_a(V, \text{Ev})$ appearing in a formula $\text{SF}_{(V, \text{Ev})}(A)$ of the $\text{Liveness}(V, \text{Ev})$ part of the TLA specification of $\text{fairexecs}(A)$, and analogously if the specification of $\text{fairtraces}(A)$ is given. (Please, notice that for a predicate $P$, $P'$ denotes its truth value in the ‘next’ state and $[N]P$ is short for $N \lor (P' \equiv P)$.) The formula is similar to the one for checking the so-called $\mu$-invariance of a predicate $\text{ENABLED}(A)_w$ for a TLA specification of an open system (Abadi and Lamport, 1994).

We have verified the externally visible behaviour of our automaton $A_1$ by checking trace inclusion in the way suggested by Propositions 1 and 2 with the TLC model checker. The latter is a part of the integrated development environment for TLA specifications, called the TLA Toolbox (2014). The specifications are actually written by using TLA$^+$ (Lamport, 2002), which is a complete formal specification language based on TLA. It complements the latter with a notation for the specification of data structures and modular specification, as well as a notation for writing hierarchically structured proofs (Lamport, 2014).

Roughly speaking, a TLA$^+$ module may contain a list of ‘imported’ modules, a declaration of module parameters, i.e. externally visible TLA constants and variables used in formulas inside the module, assumptions about the constants, definitions of symbols used in the TLA$^+$ specification, theorems expected to hold in the module under the specified
We prepared module ActOps (Fig. 2), in which Act(Ev, a) and ActInit(Ev) are defined as described in Section 4. This module can be imported by using keyword extends in the automata specification modules which need these definitions.

Formula SpecT in module A1 in Fig. 3 is the specification of traces(A1) (cf. Subsection 4.3) and SpecFT the specification of fairtraces(A1) (cf. Subsection 4.4). According to Section 4, variable s should be hidden in them, but it is not because TLC cannot handle formulas containing existential quantifier ∃. It suffices just to remember which variables are in fact internal.

It should be noticed that although A1 has a weak fairness condition on actions b and c, the latter does not guarantee action c eventually to occur because whenever c is enabled, internal action b is also enabled, and the weak fairness condition is fulfilled even if the latter always occurs. Therefore, it does not guarantee any externally visible progress of the automaton behaviour. It follows that it should be possible to prove that fairtraces(A1) = traces(A1). It should also be possible to prove that A1 externally behaves in the same way as the safe automaton, let us name it A1Req, which has the same start state and the same set of states as A1, the same input action a and output action c, but no internal actions, and the steps of which are the same as those of A1 shown in Fig. 1, except that there is no transition labelled with b. Formula Spec in module A1Req in Fig. 4 is the specification of (fair)traces(A1Req). Clearly, both A1 and A1Req induce live automata, so that we can verify them by establishing trace inclusion relations between them.

The presented modules do not only give (fair) trace specifications, but also define the sets of input (in) and output (out) actions of the automata, as well as the set of possible states (States). We followed the rule that it is useful first to specify and check the type invariant for the system being specified. An instance of module A1Req is included in module A1 and named ReqModule in order to be able to use the symbols defined in A1Req in A1. In TLA+, for an instance M, M!S refers to symbol S defined in the module of which M is an instance.

We wrote some theorems at the end of the modules, but note that for the verification with the TLC model checker, theorems need not be written because the system specification (or, generally, the antecedent of the implication stated in the theorem) and the property (the consequent of the implication) to be checked are stated in a special menu of the TLC Toolbox. We verified all the theorems with TLC. In all the theorems except those expressing the type correctness, the consequent is in fact meant to be the original formula (Spec, SpecT, or respectively SpecFT) with free variable sr replaced with a refinement mapping st, which should, according to Section 2, be a function of the variables.
EXTENDS ActOps

VARIABLES Ev, st

ReqSpec ≜ INSTANCE A1Req

vars ≜ (Ev, st)
in ≜ {⟨"a"⟩}
out ≜ {⟨"c"⟩}

ext ≜ in ∪ out

ASSUME in = ReqModule!in ∧ out = ReqModule!out

States ≜ {"s0","s1","s2"}

Init ≜ st = "s0"

InitInvariant ≜ ∧ Ev ∈ \{0","1"\} × (ext ∪ {⟨⟩}) ∧ st ∈ States

InActionA ≜ ∧ Act(Ev, ("a"))
∧ st' = if st = "s0" then "s1" else st

OutActionC ≜ ∧ Act(Ev, ("c"))
∧ (st = "s1") ∧ (st' = "s2")

IntActionBH ≜ ∧ Ev = Ev
∧ (st = "s1") ∧ (st' = st)

NextH ≜ InActionA ∨ OutActionC ∨ IntActionBH

\* LivenessH ≜ WF vars, (OutActionC ∨ IntActionBH)

LivenessH ≜ WF vars, (OutActionC) ∨ □□ ENABLED (IntActionBH)

SpecT ≜ Init ∧ □[NextH] vars

SpecFT ≜ SpecT ∧ LivenessH

ReqSpec ≜ ReqModule!Spec

\* CSpec ≜ (in = ReqModule!in) ∧ (out = ReqModule!out) ∧ ReqSpec

\* THEOREM SpecFT ⇒ □TypeInvariant
\* THEOREM SpecFT ⇒ SpecT \* fairtraces(A1) ⊆ traces(A1)
\* THEOREM SpecT ⇒ SpecFT \* traces(A1) ⊆ fairtraces(A1)
\* THEOREM SpecFT ⇒ ReqSpec \* fairtraces(A1) ⊆ (fair)traces(A1Req)

\* THEOREM SpecFT ⇒ CSpec
\* THEOREM ReqSpec ⇒ SpecFT \* (fair)traces(A1Req) ⊆ fairtraces(A1)

Fig. 3. Module A1.

of the antecedent. As the refinement mapping is simply the identity function \(\overline{st} = st\), the consequent is the same as the original formula. According to Section 2, if the implications of such formulas are valid, then also the implications of such formulas with \(st\) hidden are valid, thereby proving the trace inclusion for A1 and A1Req as stated in the comments beside the theorems in module A1 in Fig. 3, and consequently the equality of the external behaviour of automata A1 and A1Req, as well as of fairtraces(A1) and traces(A1).

We first deliberately used the wrong LivenessH formula (formula (5) from Subsection 4.4) in module A1 (the formula is shown as a line comment in Fig. 3) to check the implementation relations between automata A1 and A1Req. TLC reported an error when verifying the implication ReqSpec ⇒ SpecFT, i.e. whether traces(A1Req) ⊆ fairtraces(A1).
Fig. 4. Module A1Req.

TLC printed the error trace shown in Fig. 5. It represents exactly the trace \langle a \rangle of A1 we claim not to be allowed by the wrong specification of fairtraces(A1) in Subsection 4.4. Indeed, in this way TLC reported that the implication is not valid because trace \langle a \rangle is in the set of traces of A1Req, but not in the specified set of fair traces of A1, meaning \neg (traces(A1Req) \subseteq fairtraces(A1)). When we applied the right LivenessH formula (the uncommented one in Fig. 3), TLC reported that the implication was valid. As expected, TLC answered that implication SpecFT \Rightarrow ReqSpec was valid for SpecFT with both versions of LivenessH. Clearly, if using the wrong formula LivenessH, theorem SpecT \Rightarrow SpecFT, which asserts that traces(A1) \subseteq fairtraces(A1), is also not valid. TLC generates the same error trace as above.

According to Definition 3, the matching of input and output actions of the automata should be checked before establishing an implementation relation between them. It is easy
to see that $A_1$ and $A_1\text{Req}$ have the same sets of input and output actions. Nevertheless, module $A_1$ in Fig. 3 illustrates how it is possible to check this with TLC. This could be useful for automata with large action sets. The TLA$^+$ \texttt{assume} statement expresses the matching of the input and output action sets. Normally, an \texttt{assume} statement is used for stating assumptions about the constant parameters of a module, but it is only important that it does not contain any variables. A verification in TLC is always carried out for a particular module. When TLC is called for a verification, it first checks all the assumptions of this module. It continues only if all of them are valid, i.e. if the action sets match in our case.

Another possibility to check the matching of the action sets would be to specify it as a part of the property to be proved in the theorems expressing the trace inclusion. For example, instead of the assumption and the fourth theorem listed in $A_1$, the currently commented $\text{CSpec}$ formula and the theorem including it could be used in module $A_1$.

6. Discussion and Conclusions

The main contribution of this paper is the proposal of how to specify fair traces of fair I/O automata and how to verify the implementation relations, which is the ‘standard’ approach to the I/O automata verification, by using TLA. In this way, the specification and verification of the external behaviour of fair I/O automata can be carried out strictly formally in a single language—TLA or more precisely, TLA$^+$—and by using its tool support. In contrast to Kapus (2002, 2005), in this paper we specified the recording of action labels of I/O automata in such a way that TLA specifications of the behaviour of finite-state I/O automata cannot give infinitely many reachable states and can, therefore, be automatically verified with the TLC model checker. We defined action $\text{Act}$ in a similar way to action $\text{ChanOp}$ which is used by Ladkin et al. (1999) for the representation of message passing over channels represented by variables.

Funiak (2001) tried to apply TLA$^+$ for ordinary (i.e. not fair) I/O automata. However, he did not use TLA$^+$ directly for that model. He translated I/O automata into a state-based model by ignoring the I/O automata action labels. Müller (1998) and Søgaard-Andersen et al. (1993) considered the specification of fair I/O automata and used some kind of linear-time temporal logic. They, however, applied the temporal logic only for the specification of fairness conditions and required temporal properties of executions. The safety part of automata was specified in a semi-formal precondition/effect style. The IOA language (Garland and Lynch, 2000; Garland et al., 2003) enables formal description of ordinary I/O automata, as well as the specification of required implementation relations and state invariants. For finite-state IOA programs, a model checker exists. However, as mentioned in the introduction, verification by theorem proving cannot be carried out directly in IOA.

Systems are often developed by using stepwise refinement. First, a top-level specification is written as a composition of I/O automata (see, e.g., Müller, 1998), and a more detailed system specification is then developed by a refinement of every component of the composition. The refinement step has to be verified by checking whether the detailed system specification implements the top-level one. Generally, compositional verification is possible by establishing an implementation relation between every component in the refined specification and its counterpart in the top-level one separately. Our approach can be
used for the specification of the external behaviour of the components and the verification of trace inclusion for each one.

Sometimes, however, a system is given as a composition of I/O automata, but its requirement specification as a single one. To be able to verify trace inclusion by using our approach in such a case, a single I/O automaton should first be obtained from the components of the composition and then its traces specified by using our approach by not recording internal actions of the system. The composition of I/O automata in TLA is out of the scope of this paper, but a TLA specification of its executions could be obtained from the TLA specifications of the executions of its components in a similar way to Kapus (2009). We shall deal with the TLA specification and verification of the composition of fair I/O automata in a forthcoming paper.

TLAPS, the TLA$^+$ Proof System (2014), is being developed for writing and mechanically checking TLA$^+$ proofs entirely on the level of TLA$^+$, without the need for the user to know the mechanisms of the general-purpose theorem provers which are used behind and have also been employed for I/O automata (e.g. Garland et al., 2003; Müller, 1998). We will try to apply TLAPS for the verification of I/O automata in order to test its capabilities.

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References


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Temporalinės veiksmų logikos naudojimas teisingos įvesties/išvesties automato išorinei elgsenai specifikuoti ir tikrinti

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